## In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for forming a gate electrode for a metal oxide semiconductor device having a substrate and formed with a well and opposing trench isolation portions with a first dielectric layer formed thereon, the method comprising the steps of:

   (a) depositing a ~~relatively thin~~ first gate electrode layer of a predetermined thickness on said first dielectric layer defining an interface, ~~the thickness of said first gate electrode layer selected to minimize gate depletion adjacent said interface~~;

   (b) doping said ~~relatively thin~~ first gate electrode layer with a first dopant , defining a doped first gate electrode layer;

   (c) depositing a second gate electrode layer directly on said doped first gate electrode layer;

   (d) doping said second gate electrode layer with a second dopant defining a doped second gate electrode layer, said doped first gate electrode layer and said doped second gate electrode structure forming a structure; and

   (e) heat treating ~~the~~ said structure to activate ~~the~~ said first dopant and said second dopant ~~materials~~ with a heat treating temperature profile ~~selected to minimize diffusion of said dopant at said interface~~.

2. (Currently Amended) The method as recited in claim 1, wherein the said first gate electrode layer and said second gate electrode layer together form ~~a full thickness~~ said gate electrode.

3. (Previously Presented) The method as recited in claim 1, wherein the step of depositing a first gate electrode layer comprises depositing amorphous silicon.

4. (Previously Presented) The method as recited in claim 1, wherein the step of depositing a first gate electrode layer comprises depositing polysilicon.

5. (Previously Presented) The method as recited in claim 1, wherein the step of depositing a second gate electrode layer comprises depositing amorphous silicon.

6. (Previously Presented) The method as recited in claim 1, wherein the step of depositing a second gate electrode layer comprises depositing polysilicon.

7. (Previously Presented) The method as recited in claim 1, wherein said step of doping said first gate electrode layer comprises doping said first gate electrode layer with boron.

8. (Previously Presented) The method as recited in claim 1, wherein said step of doping said first gate electrode comprises doping said first gate electrode layer with decaborane.

9. (Previously Presented) The method as recited in claim 1, wherein said step of doping said second gate electrode layer comprises doping said second gate electrode layer with boron.

10. (Previously Presented) The method as recited in claim 1, wherein said step of doping said second gate electrode comprises doping said second gate electrode layer with decaborane.

11. (Currently Amended) A method for forming a metal oxide semiconductor (MOS) device having a substrate, comprising the steps of:

(a) forming a well and opposing trench isolation portions in said first substrate;

(b) depositing a ~~relatively thin~~ first dielectric layer thereon of a predetermined thickness; defining an interface, ~~the thickness of said first gate electrode layer selected to minimize gate depletion adjacent said interface~~;

(c) depositing a said first gate electrode layer on said first dielectric layer;

(d) doping said first gate electrode layer, defining a doped first gate electrode layer;

(e) depositing a second gate electrode layer directly on said doped first gate electrode layer;

(f) forming a gate stack from the combination of said doped first gate electrode layer and said second gate electrode layer, resulting in exposed portions of said first dielectric layer;

(g) patterning a first photoresist to expose drain extension regions on said first dielectric layer adjacent to said trench isolation portions;

(h) doping said exposed portions of said gate stack and said first dielectric layer forming drain extensions in said well between said trench isolation portions and said gate stack.

(i) removing said first photoresist and patterning a second photoresist to form spacers adjacent opposing sides of said gate stack and exposing portions of said first dielectric layer defining drain and source regions;

(j) doping said exposed portions of said first dielectric layer to form source and drain layers within said well;

(k) removing said second photoresist layer; and

(l) providing heat treatment to diffuse the implanted dopant to cause said implanted dopant to diffuse out of said first dielectric layer into said well.

12. (Previously Presented) The method as recited in claim 11, wherein said step of doping said first gate electrode layer comprises doping said first gate electrode layer with boron.

13. (Previously Presented) The method as recited in claim 11, wherein said step of doping said first gate electrode layer comprises doping said first gate electrode layer with a boron cluster implant.

14. (Previously Presented) The method as recited in claim 11, wherein said step of doping said first gate electrode layer comprises doping said first gate electrode layer with a molecular implant.

15. (Previously Presented) The method as recited in claim 11, wherein the step of doping said drain and source regions comprises doping said drain and source regions with boron.

16. (Previously Presented) The method as recited in claim 11, wherein the step of doping said drain and source regions comprises doping said drain and source regions with a boron cluster.

17. (Currently Amended) A method for forming a metal oxide semiconductor device having a substrate, comprising the steps of:

(a) forming a well and opposing trench isolations in said substrate;

(b) depositing a relatively thin first dielectric layer thereon of a predetermined thickness; defining an interface, the thickness of said first gate electrode layer selected to minimize gate depletion adjacent said interface;;

(c) depositing a first gate electrode layer directly on said first dielectric layer;

(d) forming said first gate electrode layer into a gate stack leaving exposed portions of said first dielectric layer;

(e) patterning a first photoresist layer to expose drain extension regions of said first dielectric layer;

(f) doping said drain extension regions forming drain extension layers and said well;

(g) removing said first photoresist layer;

(h) depositing a second gate electrode layer;

(i) forming said second gate electrode stack to be offset and larger than said gate stack formed from said first gate electrode layer;

(j) patterning a second photoresist layer to form spacers adjacent said second gate electrode stack to define drain and source regions;

(k) doping said drain and source regions to form drain and source layers in said well; and

(l) removing said second photoresist layer; and

(m) providing heat treatment to cause said implanted dopants to activate material implanted by said doping step.

18. (Previously Presented) The method as recited in claim 17, wherein said step of doping said drain extension regions comprises doping said drain extension regions with decaborane.

19. (Currently Amended) A method for forming a metal oxide semiconductor (MOS) device having a substrate, the method comprising the steps of:

(a) forming a well and opposing trench isolations in said substrate;

(b) depositing a first dielectric layer thereon;

(c) depositing a ~~relatively thin~~ first gate electrode layer on said first dielectric layer of a predetermined thickness; defining an interface, ~~the thickness of said first gate electrode layer selected to minimize gate depletion at said interface~~;

(d) forming said first gate electrode layer into an initial gate stack leaving exposed portions of said first dielectric layer;

(e) doping said gate stack and said exposed surfaces of said first dielectric layer;

(f) depositing a second gate dielectric layer, different than said first dielectric layer directly on said exposed surfaces of said first dielectric layer;

(g) depositing a second gate electrode deposition layer on top of said initial gate stack and said second dielectric layer;

(h) forming the second gate electrode deposition into a final gate stack;

(i) patterning a first photoresist to expose said final gate stack and drain extension regions;

(j) doping said final gate stack and said drain extension regions;

(k) removing said first photoresist;

(l) patterning a second photoresist to form side wall spacers adjacent to said final gate stack and to expose said drain and source regions;

(m) doping said drain and source regions and said final gate electrode stack to form drain and source layers in said well;

(n) removing said second photoresist layer; and

(o) providing heat treatment to activate material implanted by said doping step.

20. (Previously Presented) The process as recited in claim 19, wherein step (f) comprises implanting a species into said first dielectric layer.

21. (Previously Presented) The process as recited in claim 19, wherein step (b) comprises chemical treatment of the first dielectric layer.

22. (Previously Presented) The process as recited in claim 19, wherein step (b) comprises removal of said first dielectric layer and regrowth of a second dielectric material different from said first dielectric material.

23. (Previously Presented) The process as recited in claim 1, wherein said first and second gate electrode layers together total a thickness of a conventional gate electrode layer.

24. (Canceled)

25. (Canceled)

26. (Currently Amended) ~~The~~ A process ~~as recited in claim 24,~~ for forming a junction in a semiconductor substrate as an integral part of a semiconductor device, the process comprising the steps of:

(a) depositing a dielectric layer on said substrate;

(b) doping said dielectric layer with a first dopant type at an implant energy selected such that the dopant is contained within the dielectric layer; and

(c) providing heat treatment to cause implanted ions in said dielectric layer to diffuse into said substrate forming a junction , wherein step (b) comprises doping said dielectric layer with a series of ion implants of said first dopant type.

27. (Currently Amended) The process as recited in claim 26 ~~25~~, wherein step (b) comprises doping said dielectric layer with a boron cluster.

28. (Previously Presented) The process as recited in claim 26 wherein step (b) comprises doping said dielectric layer with a boron implant followed by a hydrogen implant.

29. (Currently Amended) The process as recited in claim 26 ~~24~~, wherein said semiconductor substrate is silicon

30. (Currently Amended) The process as recited in claim 26 ~~24~~, wherein said step (b) comprises depositing a layer of silicon dioxide.